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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,090	01/21/2005	Reinhold Berberich	502901195PUS	7011

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COHEN, PONTANI, LIEBERMAN & PAVANE
551 FIFTH AVENUE
SUITE 1210
NEW YORK, NY 10176

EXAMINER	
NGUYEN, HUNG THANH	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/522,090	BERBERICH, REINHOLD	
	Examiner	Art Unit	
	HUNG T. NGUYEN	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21/1/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24,25,27-43 and 47-52* is/are rejected.

7)☒ Claim(s) *26 and 44-46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 24-25, 27, 31-34, 38, 40, 42-43, 47-48, 50, 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Ashman et al. (US 6,142,831).

Regarding claim 24, 47: Ashman et al. discloses in figures 1 and 5, a plug device (10, see figure 1) having at least one plug element (16, see figure 1); a printed circuit board (20, see figure 5) having a circuit connected to said at least one plug element (16, see figure 5), said printed circuit board (20, see figure 5) having an external portion protruding through an opening in the electronic appliance housing (elements 16 protruding from 10, see figure 5) to an exterior of the electronic appliance housing (12) and an internal portion extending within an interior of the electronic appliance housing (element 16 appears to extend within an interior, see figure 5); and a first capacitor (30) arranged on said printed circuit board (20, see figure 5) and connected between said at least one plug element (16, see figure 5) and a potential of the electronic appliance housing (cover of 10), said at least plug element (16, see figure 1) being conductively connected to said first capacitor (16 and 30 connected, see figure 5) and said circuit at said external portion of said printed circuit board (20, see figure 5).

Regarding claim 25, 27, 43, 48, 50: Ashman et al. discloses in figure 5, the first capacitor (explain above) comprises first (portion of 36) and second (portion of 38) capacitor faces and an insulating layer (insulation layer should be between 36, 38 and not shown in figure), said first (portion of 36) and second (portion of 38) capacitor faces being arranged opposite one another such that they are separated by said insulating layer, said first capacitor face being conductively connected to the potential of the electronic appliance housing (36 appears to connect to the housing) and said second (38 appears to connect to 32) capacitor face being conductively connected to said circuit (portion 32).

Regarding claim 31: Ashman et al. discloses in figure 5, at least one of said first (explain above) and second (explain above) capacitor faces includes a capacitor coating (40) on the printed circuit board (explain above).

Regarding claim 32, 33: Ashman et al. discloses in figure 5, the signal lines (portion of 40 connecting 16, 30, 40, 32) connecting said circuit to one of said at least one plug element and said second capacitor face.

Regarding claim 34, 42: Ashman et al. disclose in figure 5, printed circuit board is dimensioned and arranged such that said printed circuit board is tightly enclosed in the opening in the electronic appliance housing (element 20 is enclosed in element 10).

Regarding claim 38: Ashman et al. discloses in figure 1, the connecting element comprises a rivet (16 appears to be rivet).

Regarding claim 40, 52: Ashman et al. discloses in figure 1, the printed circuit board defines cutouts (cutout portion locate in front of 10) arranged and dimensioned for

receiving corresponding portions of the opening region of the electronic appliance housing with a press fit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28-30, 35-37, 39, 41, 49, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashman et al. (US 6,142,831) in view of Pfeifer (US 5,152,699).

Regarding claim 28, 35: Ashman discloses all elements of the interference suppression device as described above with respect to claim 27 except, Ashman et al. does not disclose a second capacitor including third and fourth capacitor faces which lie one above the other and which are electrically insulated from one another, said third capacitor face being conductively connected to said at least one plug element and said fourth capacitor face being conductively connected to the electronic appliance housing potential.

Pfeifer discloses in figure 1, a second (44, second from bottom) capacitor including third (44, third from bottom) and fourth (44, fourth from bottom) capacitor faces which lie one above the other and which are electrically insulated from one another, said third capacitor face being conductively connected to said at least one plug element and said

fourth capacitor face being conductively connected to the electronic appliance housing potential (44 were being electrically insulate and on top each other).

Ashman et al. and Pfeifer are analogous art because they are from the same field of endeavor to make connectors.

Therefore, it would have been obvious for one ordinary skill in the art at the time of the invention to make connector of Ashman et al. to have various capacitors as taught by Pfeifer for the benefit of filtering various plug elements.

Regarding claim 29: Ashman et al. discloses all elements of the interference suppression device as described above with respect to claim 28 except, Ashman et al. does not disclose the fourth capacitor face is arranged on a surface of said printed circuit board.

Pfeifer discloses in figure 1, the fourth capacitor (explain above) face is arranged on a surface of said printed circuit board (elements 28, 30, 36, 44).

Ashman et al. and Pfeifer are analogous art because they are from the same field of endeavor to make connectors.

Therefore, it would have been obvious for one ordinary skill in the art at the time of the invention to make connector of Ashman et al. to have fourth capacitors as taught by Pfeifer for the benefit of filtering various plug elements.

Regarding claim 30, 37: Ashman et al. discloses all elements of the interference suppression device as described above with respect to claim 28 except, Ashman et al. does not disclose the first and fourth capacitor faces are conductively connected by

plated through holes with enclose between them the second and the third capacitor faces and extend approximately on the plane of the housing wall.

Pfeifer discloses in figure 1, the first and fourth capacitor faces are conductively connected by plated through holes (holes allow pin 16 goes through) with enclose between them the second and the third capacitor faces and extend approximately on the plane of the housing wall (see figure 1).

Ashman et al. and Pfeifer are analogous art because they are from the same field of endeavor to make connectors.

Therefore, it would have been obvious for one ordinary skill in the art at the time of the invention to make connector of Ashman et al. to have holes as taught by Pfeifer for the benefit of allowing pin to pass through.

Regarding claim 36, 49: Ashman et al. discloses all elements of the interference suppression device as described above with respect to claim 35 except, Ashman et al. does not disclose at least on of said first and fourth capacitor faces in arranged such that the electronic appliance housing bears resiliently against said at least one of said first and fourth capacitor faces proximate the opening.

Pfeifer discloses in figure 1, at least on of said first and fourth capacitor faces in arranged such that the electronic appliance housing bears resiliently (pin 16 appears to be resilient) against said at least one of said first and fourth capacitor faces proximate the opening.

Ashman et al. and Pfeifer are analogous art because they are from the same field of endeavor to make connectors.

Therefore, it would have been obvious for one ordinary skill in the art at the time of the invention to make connector of Ashman et al. to have resilient as taught by Pfeifer for the benefit of allowing pin to connect.

Regarding claim 39, 51: Ashman et al. discloses all elements of the interference suppression device as described above with respect to claim 28 except, Ashman et al. does not disclose the printed circuit board is arranged and dimensioned so that one of said first and fourth capacitor faces is connectable to the electronic appliance by an interlocking connection.

Pfeifer discloses in figure 1, the printed circuit board is arranged and dimensioned so that one of said first (explain above) and fourth (explain above) capacitor faces is connectable to the electronic appliance by an interlocking connection (see figure 1).

Ashman et al. and Pfeifer are analogous art because they are from the same field of endeavor to make connectors.

Therefore, it would have been obvious for one ordinary skill in the art at the time of the invention to make connector of Ashman et al. to have interlock connection as taught by Pfeifer for the benefit of connecting components to board/pins.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashman et al. (US 6,142,831) further in view of Clyatt, III (US 5,865,648).

Regarding claim 41: Ashman et al. discloses all elements of the interference suppression device as described above with respect to claim 25 except, Ashman et al.

does not disclose one of an adhesive bond and solder connection for conductively connecting said first capacitor face to the electronic appliance housing.

Clyatt, III discloses one of an adhesive bond and solder connection for conductively connecting said first capacitor face to the electronic appliance housing (see column 6).

Ashman et al. and Clyatt, III are analogous art because they are from the same field of endeavor to make connectors.

Therefore, it would have been obvious for one ordinary skill in the art at the time of the invention to make connector of Ashman et al. to have adhesive bond as taught by Clyatt, III for the benefit of connecting components.

Allowable Subject Matter

Claims 26, 44-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 26: Ashman discloses all elements as of interference device as described above with respect to claim 25 except, Ashman does not disclose the insulating layer is formed by a portion of said printed circuit board. There would be no motivation to make this modification.

Regarding claims 44-46: Ashman et al. discloses all elements of the interference suppression device as described above with respect to claim 24 except, Ashman does not disclose the shielding arm lying adjacent to one another. There would be no motivation to make this modification.

Relevant Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Ashman et al. (US 6,142,831) teaches the multifunction connector, Clyatt, III (US 5,865,648) teaches the electronic connector, Pfeifer (US 5,152,699) teaches the filter connector, Farrar et al. (US 4,820,174) teaches the modular connector, Reider et al. (US 5,509,825) teaches connector filter pack, Plass (US 5,242,318) teaches electronic signal lines, Dingenotto et al. (US 6,506,079) teaches the connecting device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG T. NGUYEN whose telephone number is 571-272-5983. The examiner can normally be reached on 8:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, REICHARD DEAN can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

HN

Hung Thanh Nguyen 9/27/06

DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800 9/29/06